

Figure 1. Bootstrap circuit used in our current design

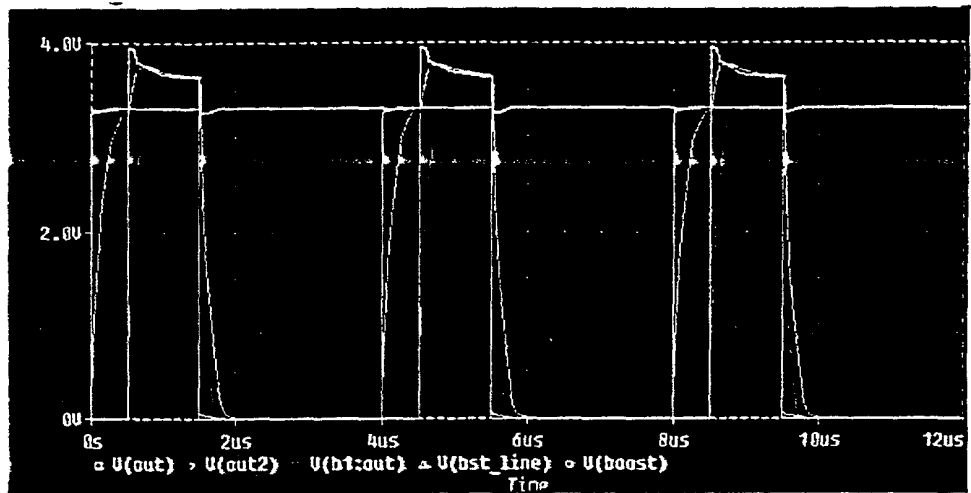


Figure 2. Simulation results from current bootstrap circuit

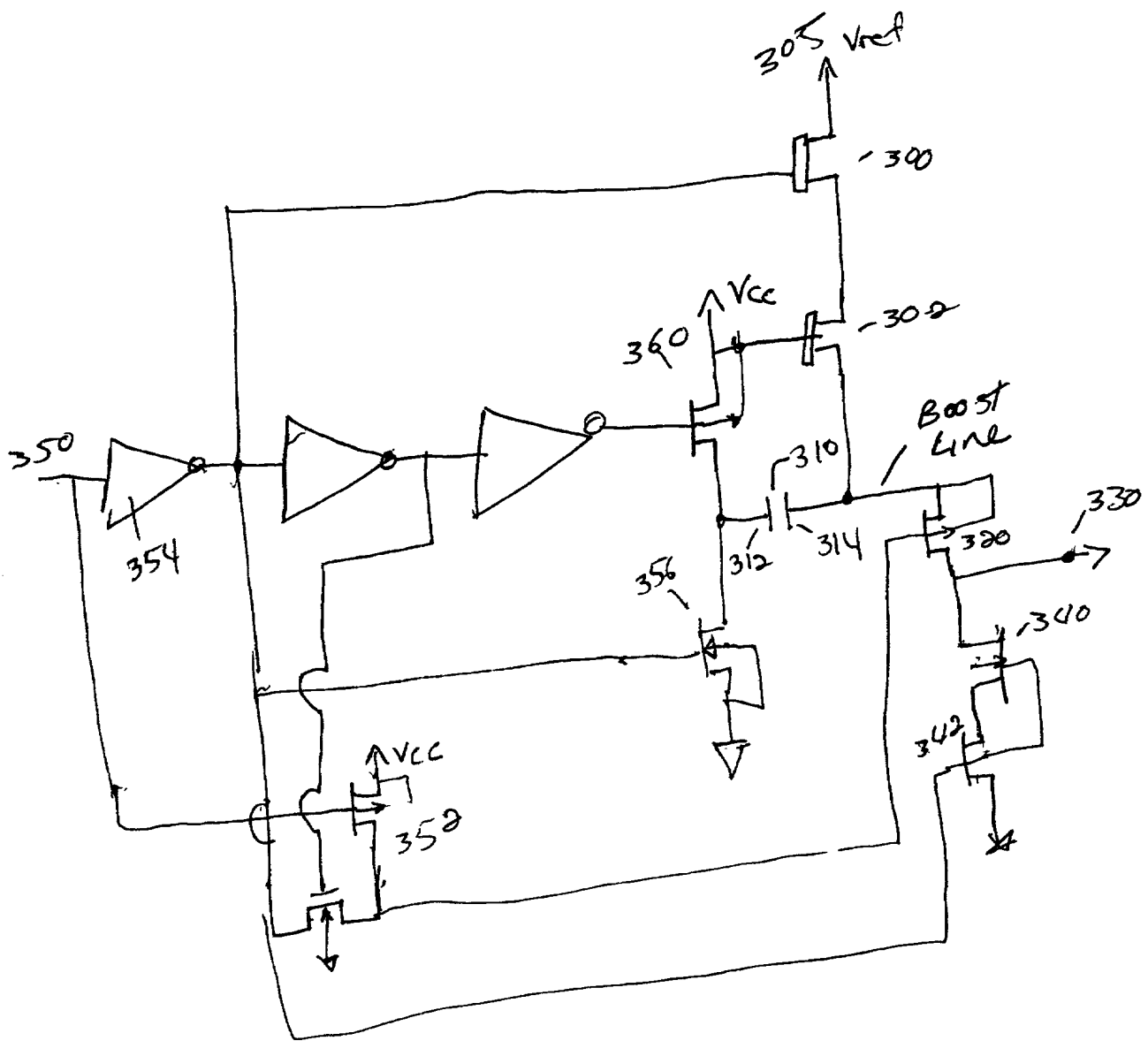


FIG 3

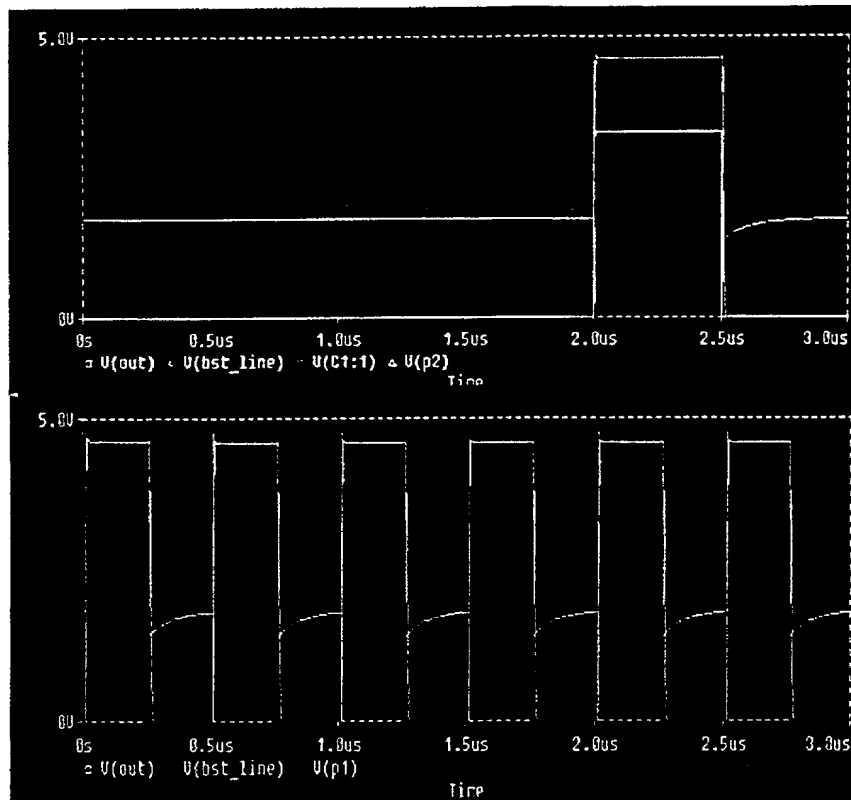


Figure 7. Simulation for single and continuous clock boosting signals

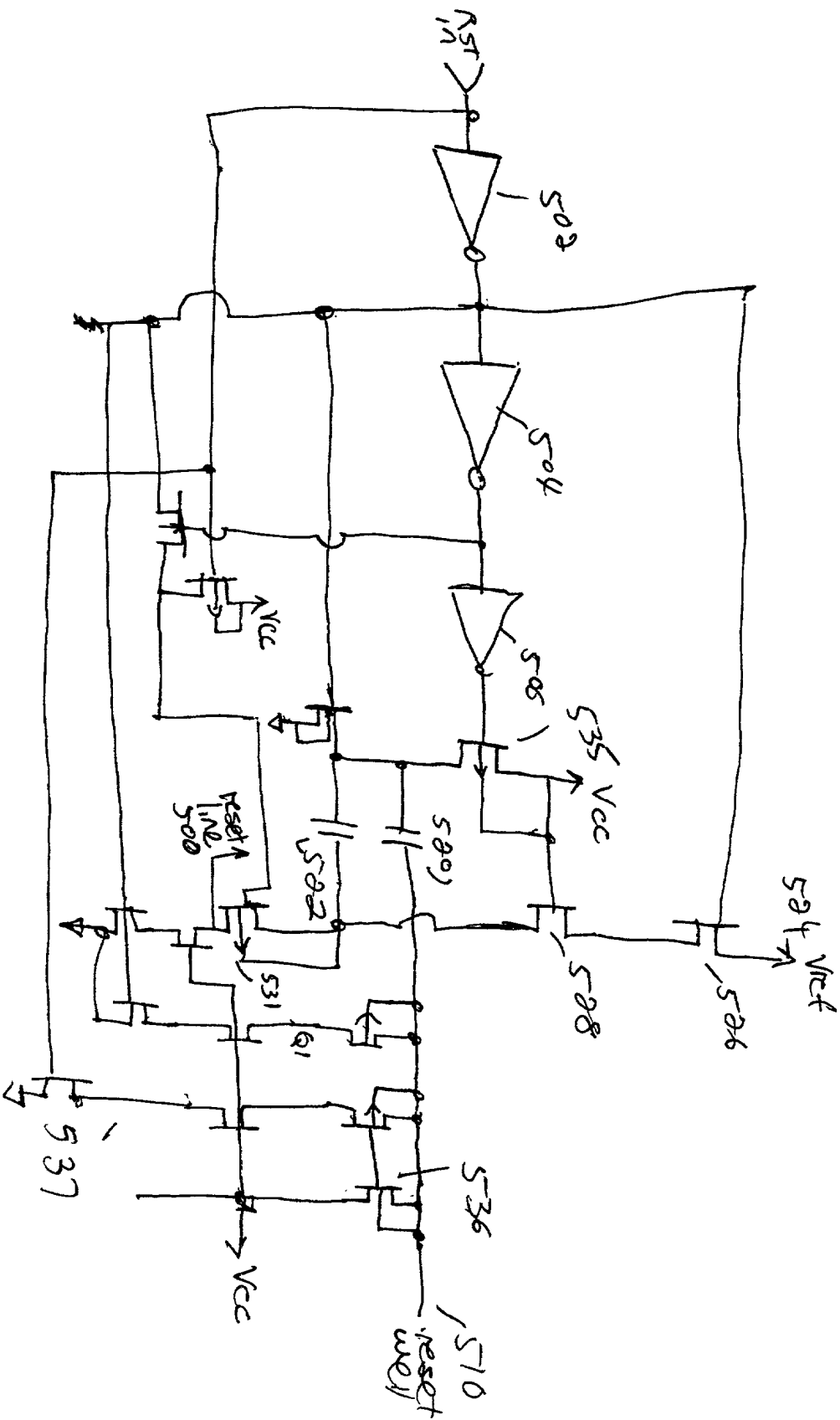


FIG 5

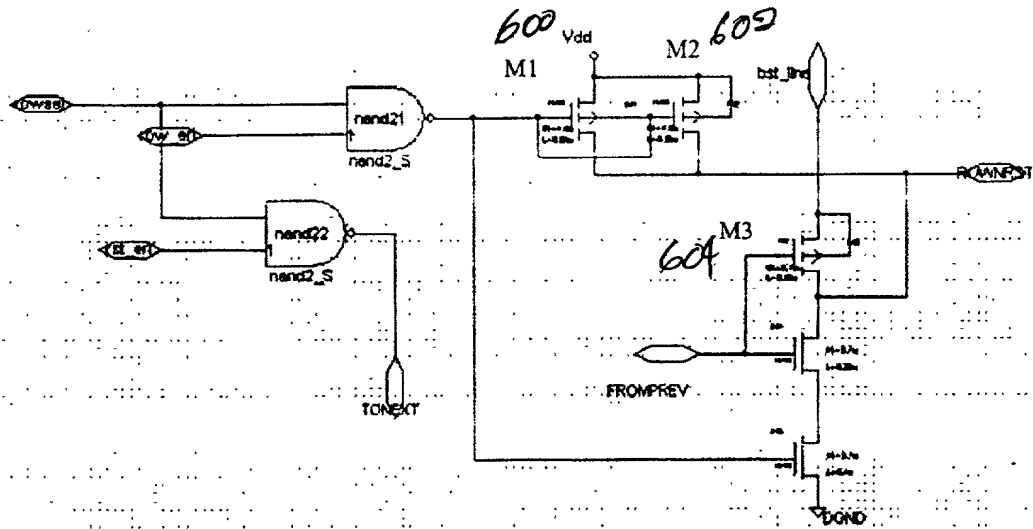
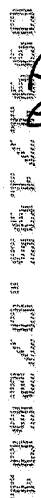


Figure 6 Current used row driver for shared ROW and boosting RST



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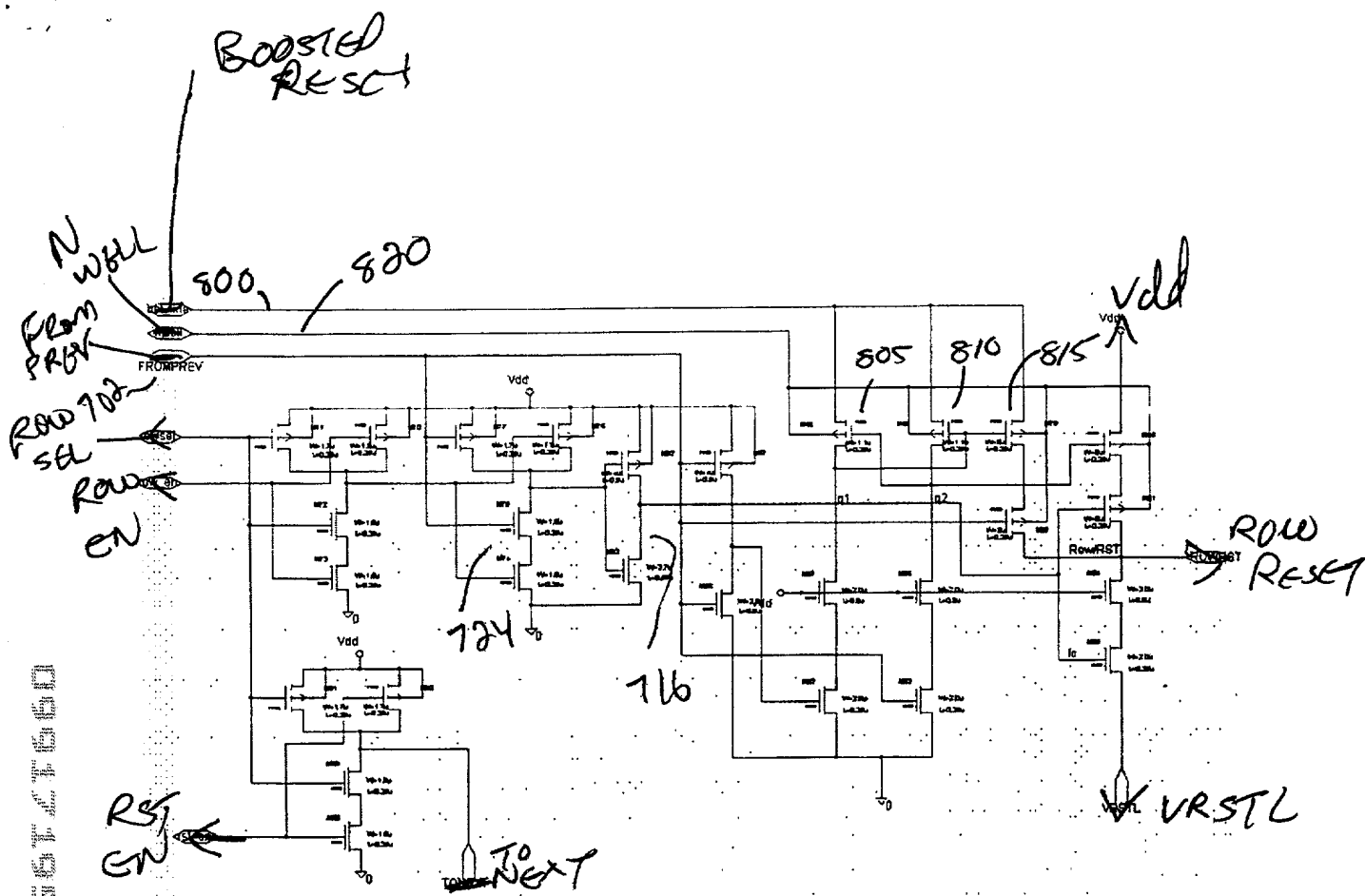


Figure 8. New row driver with separate boosting for RST and N-well



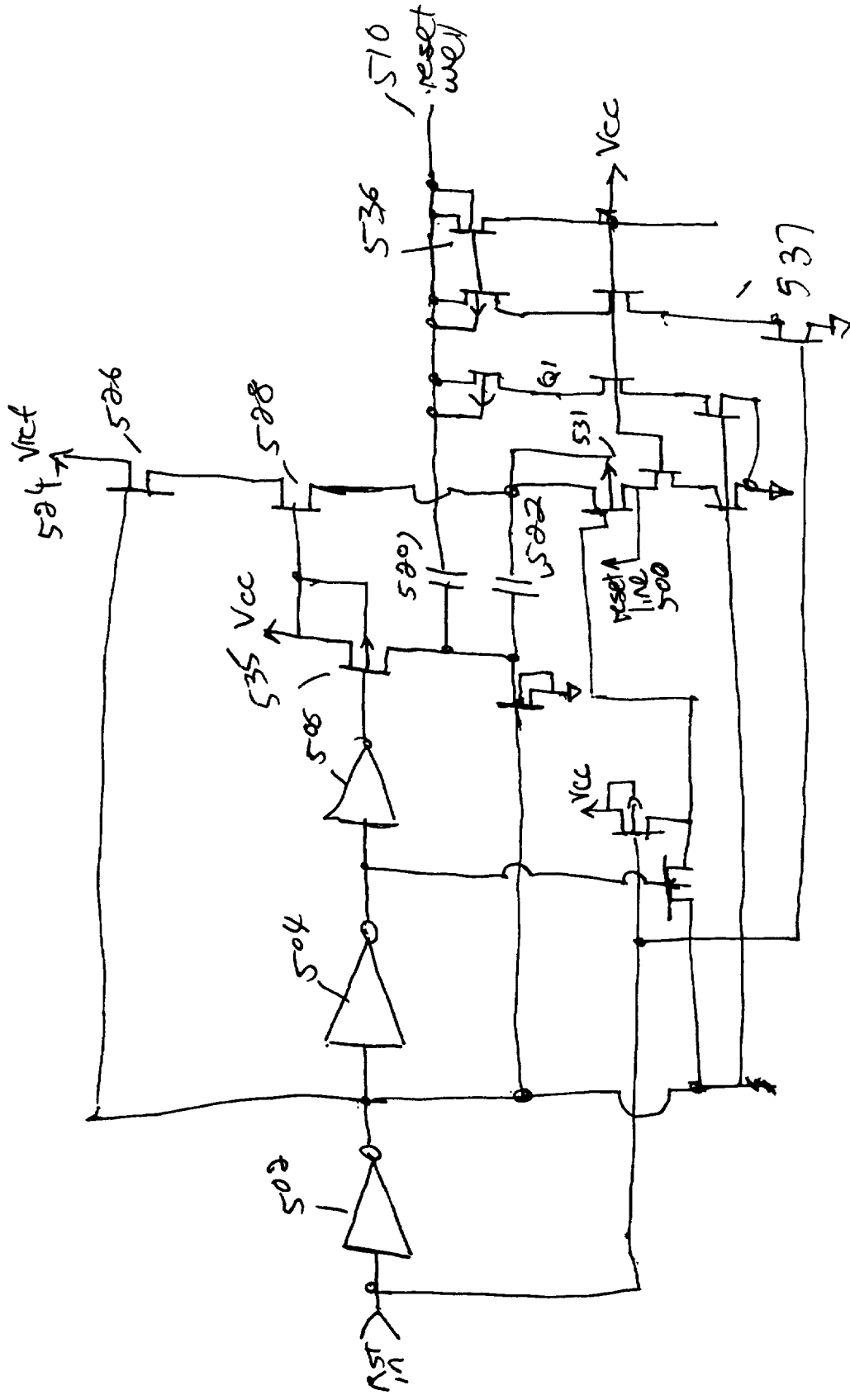


FIG 5